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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/385,666	08/26/1999	ROBERTO SUAYA	002282.P066	9500

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2123	21

DATE MAILED: 12/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PAG

Office Action Summary

Application No.	Applicant(s)
09/385,666	Suaya And Gabillet
Examiner	**Art Unit**
Thai Phan	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Aug. 22 , 2003 and Oct. 28, 2003* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *15-57* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *15-57* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to a CPA filed on Aug. 22, 2003 and compliant amendment filed on Oct. 27, 2003. Claims 15-57 are pending.

Drawings

1. Acknowledgment has been made for drawing correction changes.

Information Disclosure Statement

2. The information disclosure statement filed 02/19/2003 has been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 15-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen, James, US patent no. 6,300,765 B2.

As per claim 15, Chen anticipates method and system for measuring cross-coupling capacitances in an integrated circuits with feature limitations as claimed (Abstract and Summary of the Invention). According to Chen, the measurement method includes steps

Providing at least first and second wires in a wire interconnection structure (col. 3, lines 10-28), charging interconnect wiring to a predetermined voltage by charging means (col. 3, lines 51-63),

Performing a first measurement associated with a capacitance of the first wire (col. 5, lines 33-45),

Charging the second wire to the predetermined voltage, discharging (recharging) the first wire to the predetermined voltage, performing a second measurement associated with a capacitance of the first wire, and calculating a charge difference between the first and second measurement due to charge induced on the target interconnect to determine the cross-coupling capacitance between the first and second wire controlling by frequency control voltage (Background of the Invention, col. 5, line 5 to col. 7, line 33).

As per claim 16, Chen anticipates coupling series transistor with configuration as claimed (Fig. 1).

As per claim 17, Chen anticipates applying periodic signals to the transistor gates as claimed (Fig. 1).

As per claim 18, Chen anticipates applied signals are periodic and synchronous or not simultaneous (Fig 3, col. 5, line 33 to col. 6, line 55).

As per claim 19, Chen anticipates charging and discharging interconnection wires in order.

As per claim 20, Chen anticipates measuring cross-coupling capacitances for multiple wire interconnections (Figs. 1-3, cols. 5 and 6).

As per claims 21-22, Chen anticipates means for measuring cross coupling capacitances for multiple neighbor wires and using the same measurement techniques for wire neighbor.

As per claim 23, Chen uses transistors in conjunction with transmission wire for measurement.

As per claims 24-25, Chen anticipates capacitance measurement for wires in multilayer integrated circuit, repeating the measurement over a number of cycle over a timing diagram to compute a correct measurement (cols. 5-6).

As per claims 26 and 27, Chen anticipates measuring charge and current for capacitance measurement.

As per claims 28-31, Chen anticipates logic inverter connected between transmission wires for the test interconnect charging circuit (Fig. 1, block (117)).

As per claim 32, Chen anticipates charging mechanism as claimed for capacitance measurement, namely, charging transmission wire for a cycle time period, discharging or recharging for other time cycle depending on charge cycle process, measuring rate of discharging and coupling capacitance (col. 5, lin 35 to col. 7, line 18).

As per claims 33-34, Chen anticipates transistor in conjunction with transmission wires and effect of neighbor wires in capacitance measure.

As per claim 35, Chen anticipates method and system for measuring cross-coupling capacitances in an integrated circuits with feature limitations as claimed (Summary of the Invention). According to Chen, the measurement method includes means for providing a first and second transistors coupled in series (Fig. 1), means for providing at least first and second wires in a wire interconnection structure (col. 3, lines 10-30), charging interconnect wiring to a predetermined voltage by charging means (col. 3, lines 59-65), performing a first measurement associated with a capacitance of the first wire (col. 5, lines 35-59), charging the second wire to the predetermined voltage, discharging or recharging the charged first wire to the predetermined voltage, performing a second measurement associated with a capacitance of the first wire, and calculating a difference between the first and second measurement (substraction) due to charge induced or relative charge induced on the target interconnect to determine the cross-coupling capacitance between the first and second wire as claimed (Background of the Invention, col. 5, line 5 to col. 7, line 33).

As per claim 36, Chen anticipates low/high logic values feature as claimed.

As per claims 37-38, Chen anticipates a logic coupled to the interconnection wires such logic including inverter, gates, etc. as claimed (Figs. 1-3).

As per claims 39-41, Chen anticipates the claimed limitations for measurement of cross-coupling capacitance. Such features include a plurality of periodic signals are used to control charging the first wire and periodic signal is used to control the charging of the second wire (Fig. 3).

As per claim 42, Chen anticipates ammeter for measuring cross-coupling capacitances.

As per claim 43, Chen anticipates measurement of cross-coupling capacitance for multiple neighbor wires to the first wire.

As per claim 44, Chen anticipates means for measuring cross coupling capacitances for multiple neighbor wires and using the same measurement techniques for wire neighbor.

As per claims 45-46, Chen anticipates capacitance measurement for wires in multilayer integrated circuit, repeating the measurement over a number of cycle over a timing diagram to compute a correct measurement and the measurement is accomplished with library element or with measurement tools (cols. 5-6).

As per claim 47, Chen anticipates method and system for measuring cross-coupling capacitances in an integrated circuits with feature limitations as claimed (Summary of the Invention). According to Chen, the measurement method includes means for providing a first and second transistors coupled in series (Fig. 1), means for providing at least first and second wires in a wire interconnection structure (col. 3, lines 10-30), charging interconnect wiring to a predetermined voltage by charging means (col. 3, lines 59-65), performing a first measurement associated with a capacitance of the first wire (col. 5, lines 3559), charging the second wire to the predetermined voltage, discharging or recharging the charged first wire to the predetermined voltage, usually at lower voltage level, performing a second measurement associated with a capacitance of the first wire, and calculating a charge difference or relative charge induced on the target interconnect (col. 6, lines 22-56, for example) between the first and second measurement to determine the cross-coupling capacitance of the interconnect wires claimed (Background of the Invention, col. 5, line 5 to col. 7, line 33).

As per claims 48-50, Chen anticipates such feature limitations for cross-coupling capacitance measurement.

As per claim 51, Chen anticipates method and system for measuring cross-coupling capacitances in an integrated circuits with feature limitations as claimed (Summary of the Invention). According to Chen, the measurement method includes means for providing a first and second transistors coupled in series (Fig. 1), means for providing at least first and second wires in a wire interconnection structure (col. 3, lines 10-30), charging interconnect wiring to a predetermined voltage by charging means (col. 3, lines 59-65), performing a first measurement associated with a capacitance of the first wire (col. 5, lines 35-59), charging the second wire to the predetermined voltage, discharging or recharging the first wire which was charged before) to the predetermined voltage at lower voltage level, performing a second measurement associated with a capacitance of the first wire, and calculating a difference between the first and second measurement (substraction) to determine the cross-coupling capacitance between the first and second wire as claimed (Background of the Invention, col. 5, line 5 to col. 7, line 33).

As per claim 52, Chen anticipates ammeter being used to measure current for capacitance measurement by taking more than one measurement of current through the interconnect wires while the wires are both charges to a predetermined voltage, and a measurement of current through the first wire while the first wire charged to a predetermined voltage and the second wire is discharged to ground (Fig. 3, cols. 5-7).

As per claims 53-54, Chen anticipates cross-coupling capacitance in multiple neighbor wires or interconnection wires.

As per claim 55, Chen anticipates multilayer interconnection in an integrated circuit under capacitance measurement.

As per claim 56, Chen anticipates inverter in conjunction with interconnection wires for capacitance measurement (Fig. 1, cols. 4-6).

As per claim 57, Chen anticipates timing for charging and transistors are not activated simultaneously as claimed (cols. 5-6).

Response to Arguments

5. Applicant's arguments in amendment filed Aug. 22 and Oct. 27, 2003 have been fully considered but they are moot in view of a new ground of rejection.

In response to applicants' argument on amendment, filed on Aug. 22, 2003, Chen does not take more than one measurement in determining cross-coupling capacitance (page 10), the examiner responds such argued feature is anticipated in Chen. For example, Chen requires measurement of current for CHRG1 is high (col. 6, lines 32-43), current measurement for charging control signals CHRG2 and CHRG1 are high (col. 6, lines 44-56), measurement for CHRG2 is high and control signals DCHRG2, CHRG1 and SCHRG1 are low (col. 6, lines 57-62). Chen thus takes more than one measurement to determine cross-coupling capacitances.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this final action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306, (for Formal communications; please mark "EXPEDITED PROCEDURE"),

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

December 1, 2003

Thaiphan
Patent Examiner
Thai Phan
AU : 2123